



“Energy Efficient Signal Processing “

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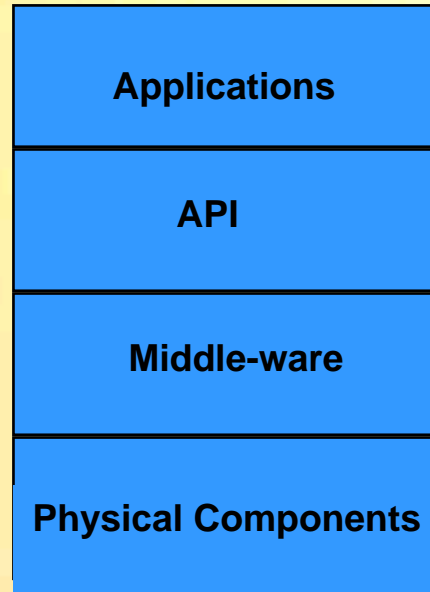
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- Algorithms
- Soft-Ware
- System Architecture
- Device Architecures & Technologies
- Summary

The Problem

- It is a challenge to design a digital signal processing systems with heavy loads consuming only microwatts of power.
- So far semiconductor technology improvements such as reduction of supply voltage & geometry has helped.

System Structure



Holistic System View

Algorithms

FFT

Filter

Mult. EQ, Sync..

Coders

Prot.

Software

Language

Code writing style

Compiler

SW Architecture

Low power System



System Architecture

Von Neumann (CPU, RAM & prog)

Paralellism

DSP (Pipelining)

Device Architecture & technology

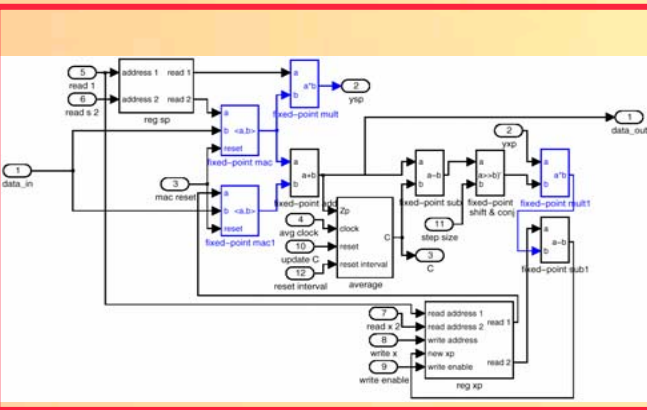
C-MOS (15-30 nm 1.3 V)

Super-conducting & Quantum Computing

DSPs, FPGAs & Logic

What is really happening...

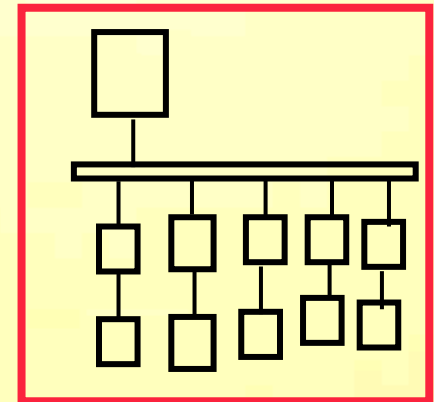
Starting with a parallel algorithmic description



Re-entering it using a sequential description

```
While (i=0;i++;i<num) {  
    a = a * c[i];  
    b[i] = sin (a * pi) +  
           cos(a*pi);  
};  
Outfil = b[i] * indata;
```

Then try to rediscover the parallelism

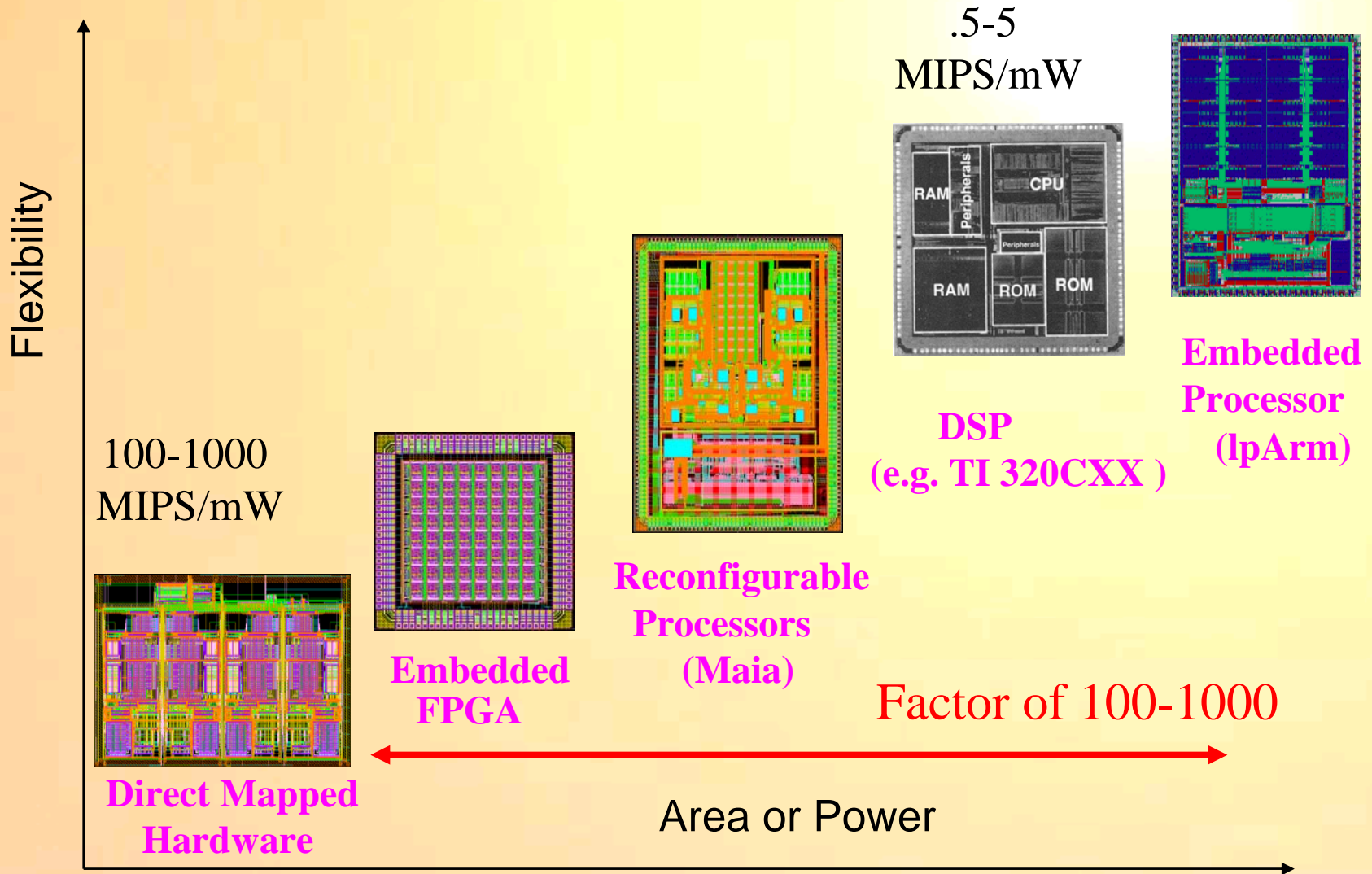


*We take this path so that we can use an architecture that is orders of magnitude less efficient in area and power
???????*

Activities that alone or collectively can contribute to power reduction

- **Algorithms and software optimized for a target architecture**
- **Develop algorithms that avoid massive shuffling of data between memory and CPU**
- **Consider strength and weakness in the target architecture when writing code**
- **A DSP is a sequence machine extremely fast for dedicated tasks and allow pipelining**
- **Dedicated hardware for certain time critical functions (multiplication and FFT)**
- **General u-processors are slow & power hungry in execution of DSP algorithms**
- **DSPs offer the possibility to turn of the clock partially when a task is completed.**
- **Consider gated clocks.**

Different architectures have very different efficiencies ...



DSP Implementation Alternatives

ASIC

FPGA

**STD
DSP**

Flexibility

Perf. Speed

Area/Cost

Vendor Independence

SW dev. Effort

HW Design Effort



- View The Problem From Application & System Level
- Specify Application- Specific Performance Needs
- What algorithms & Architectures are essential to achieving these performance goals?
- Establish a balance between functionality, energy consumption, latency, flexibility and robustness.
- **Low power means power minimization for Algorithms, Architectures in both SW & HW (Protocols)**
- Explore cortical dynamics, network architecture and algorithms and derive principles to inspire the electronic society.

**Thank
You**

for listening

Power dissipation in processors

Average temp/cm²

